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EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,425	KACZYNSKI, BRIAN J.	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *1-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11022004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 1-23 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected claims, there being no allowable generic or linking claim. Election was made **without** traverse in the reply by a phone call on October 28, 2004 at 4:57 by Mr. Mark J. Danielson ((650) 233-4777) attorney of the applicants.

Drawings

The drawings are objected to under 37 CFR 1.83(b) because they are incomplete. 37 CFR 1.83(b) reads as follows:

> When the invention consists of an improvement on an old machine the drawing must when possible exhibit, in one or more views, the improved portion itself, disconnected from the old structure, and also in another view, so much only of the old structure as will suffice to show the connection of the invention therewith.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled

"Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: **DP and DN** (page 11 line 21 of the disclosure);**142- to 142-n** (page 12 line 12 of the disclosure); **160-1 to 160-n** (page 12 line 13 of the disclosure); **160-1** (page 13 line 14 of the disclosure**); OUTN and OUTP** (page 14 line 7 of the disclosure); **OUTN and OUTP** (page 14 line 8 of the disclosure); **160'** (page 14 line 13 of the disclosure). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to because the hand written number and the deleted block names doesn't help to understand the invention, It is suggested to improve and correct the drawing; in figure 4 the block that seems to be 160 id the switch network plus the gain cell, but the disclosure uses 160 only for the gain cell. Corrected drawing

sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

Page 2 line 16 the recitation "CDMA" is not spell out. Is suggested to be changed to "Code Division Multiple Access (CDMA)".

Page 3 line 4 the recitation "Federal Communication Commission" is used later on in the disclosure only with the initials (page 8 line 2 and page 10 line 1), for that reason is suggested to be changed to "Federal Communication Commission (FCC)".

Page 6 line 13 the recitation "upmixer 130" is not correct. Is suggested to be changed to "upmixer 110".

Page 6 line 13 the recitation "variable gain amplifier" is used later on in the disclosure only with the initials (page 9 line 9), for that reason is suggested to be changed to "variable gain amplifier (VGA)".

Page 6 line 14 the recitation "0dB to 15.5dB" is suggested to be changed to "0 dB to 15.5 dB".

Page 6 line 15 the recitation "0.5dB" is suggested to be changed to "0.5 dB".

Page 7 line 14 the recitation "130desirable" is suggested to be changed to "130 desirable".

Page 9 line 6 the recitation "0.8□s" is not understood, it seems to mean "0.8 μs".

Page 9 line 7 the recitation "4□s" is not understood, it seems to mean "4 μs".

Page 9 line 11 the recitation "amplifier130" is suggested to be changed to "amplifier 130".

Page 9 line 19 the recitation "0.5dB" is suggested to be changed to "0.5 dB".

Page 9 line 21 the recitation "2.0dB" is suggested to be changed to "2.0 dB".

Page 10 line 2 the recitation "2us in 62.5ns" is suggested to be changed to "2 μs in 62.5 ns".

Page 11 line 21 the recitation "DP (positive) and DN (negative)" is not shown in figure 3.

Page 11 line 22 the recitation "PMOS" is not spell out. Is suggested to be changed to "p-type metal-oxide-semiconductor (PMOS)".

Page 12 line 2 the recitation "VDD-referenced" is suggested to be changed to "Voltage Drain-Drain (VDD) referenced"

Page 12 line 3 the recitation "NMOS" is not spell out. Is suggested to be changed to "n-type metal-oxide-semiconductor (NMOS)".

Page 12 line 12 the recitation "142-1 to 142-n" is not shown in figure 4.

Page 12 line 13 the recitation "160-1 to 160-n" is not shown in figure 4.

Page 12 line 20 the recitation "GN" is suggested to be changed to "gn" as shown in the graphic.

Page 12 line 21 the recitation "GP" is suggested to be changed to "gp" as shown in the graphic.

Page 13 line 6 the recitation "POST_B" is suggested to be changed to "pos_b" as shown in the graphic.

Page 13 line 7 the recitation "NEG_B" is suggested to be changed to "neg_b" as shown in the graphic (twice).

Page 13 line 7 the recitation "POST_B" is suggested to be changed to "pos_b" as shown in the graphic.

Page 13 line 14 the recitation "160-1" is not shown in figure 4.

Page 13 line 16 the recitation "INP" is suggested to be changed to "inp" as shown in the graphic.

Page 13 line 16 the recitation "INN" is suggested to be changed to "inn" as shown in the graphic.

Page 13 line 19 the recitation "GP" is suggested to be changed to "gp" as shown in the graphic.

Page 13 line 20 the recitation "GN" is suggested to be changed to "gn" as shown in the graphic.

Page 13 line 21 the recitation "POST_B" is suggested to be changed to "pos_b" as shown in the graphic.

Page 13 line 21 the recitation "NEG_B" is suggested to be changed to "neg_b" as shown in the graphic.

Page 14 line 6 the recitation "GP" is suggested to be changed to "gp" as shown in the graphic.

Page 14 line 6 the recitation "GN" is suggested to be changed to "gn" as shown in the graphic.

Page 14 line 7 the recitation "GP" is suggested to be changed to "gp" as shown in the graphic.

Page 14 line 7 the recitation "GN" is suggested to be changed to "gn" as shown in the graphic.

Page 14 line 7 the recitation "OUTN" is not shown in figure 4.

Page 14 line 7 the recitation "OUTP" is not shown in figure 4.

Page 14 line 8 the recitation "OUTN" is not shown in figure 4.

Page 14 line 8 the recitation "OUTP" is not shown in figure 4.

Page 14 line 13 the recitation " 160' "is not shown in figure 4.

Page 14 line 18 the recitation "0.5dB, 1.0dB, 1.5dB, 2.0dB and 3.0dB" is suggested to be changed to "0.5 dB, 1.0 dB, 1.5 dB, 2.0 dB and 3.0 dB"

Page 14 line 19 the recitation "POST_B" is suggested to be changed to "pos_b" as shown in the graphic.

Page 14 line 19 the recitation "NEG_B" is suggested to be changed to "neg_b" as shown in the graphic.

Appropriate correction is required.

Claim Objections

Claims 24 are objected to because of the following informalities:

In claim 4 line 4 the recitation "VDD-referenced" is indefinite, it is suggested to be changed to "Voltage Drain-Drain (VDD) referenced"

In claim 26 line 2 the recitation "NMOS" is indefinite, it is suggested to be changed to "n-type metal-oxide-semiconductor (NMOS)"

In claim 29 line 2 the recitation "PMOS" is indefinite, it is suggested to be changed to "p-type metal-oxide-semiconductor (PMOS)"

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 24, 25, 26, 27 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jett et al. (US 4520324), and further in view of Vagher (US 5313172).

As per claim 24 Jett et al. (US 4520324) discloses a variable gain amplifier including an inductively loaded folded cascode circuit that inputs an input differential signal having a referenced output level and outputs a current (figure 3 block 19, column 3 line 34); an input current load circuit that inputs the current from the inductively-loaded folded cascode circuit and outputs an output differential signal having a ground-referenced output level (figure 3 blocks 21 and 21', column 3 line 37). Jett et al. (US 4520324) doesn't disclose a plurality of gain cells and a plurality of switches. Vagher (US 5313172) discloses a digitally switched gain amplifier with a plurality of gain cells, each gain cell coupled to the input current load circuit and receiving the output differential signal, each gain cell comprising two current mirror circuits (figure 3 blocks Q30/Q32 and Q34/Q36, column 4 lines 65-69); and a plurality of switching circuits, each switching circuit coupled to one of the plurality of gain cells and each switching circuit operating in a positive mode and in a negative mode, the negative mode having an opposite polarity to the positive mode, and wherein the plurality of switching circuits operate to place more of the plurality of gain cells in the positive mode than in the negative mode (figure 3 blocks Q20-Q25, column 4 lines 60-64). The MOS gain controlled amplifier disclosed by Jett et al. (US 4520324) can be combined to supply current to the digitally switched gain amplifier for digitally controlled automatic gain control amplifier applications disclosed by Vagher (US 5313172). It would have been obvious to one of ordinary skill in the art at the time the invention was made in order to

reduce the high-frequency noise in the incoming current signal for the digitally switched gain amplifier disclosed by Vagher (US 5313172), to use the MOS gain controller amplifier proposed by Jett et al. (US 4520324).

As per claim 25, Vagher (US 5313172) and Jett et al. (US 4520324) teach claim 24, Vagher (US 5313172) discloses that a positive mode and the negative mode occur at the same time in a gain cell of the variable gain amplifier, thereby providing for fine gain adjustments (figure 3 blocks $+V_{IN}$ and $-V_{IN}$).

As per claim 26, Vagher (US 5313172) and Jett et al. (US 4520324) teach claim 24, Jett et al. (US 4520324) disclose a input current load circuit comprised of four NMOS transistors arranged in a cascode configuration (figure 3 blocks I3, I3', I2, and I2', column 3 line 38).

As per claim 27, Vagher (US 5313172) and Jett et al. (US 4520324) teach claim 26. Jett et al. (US 4520324) outputs 21 and 21' are connected to the VCA1 and VCA2 of Vagher (US 5313172) and the input current load circuit is mirrored by each of the plurality of gain cells.

As per claim 30, Vagher (US 5313172) and Jett et al. (US 4520324) teach claim 24. Jett et al. (US 4520324) outputs 21 and 21' are connected to the VCA1 and VCA2 of Vagher (US 5313172) and the input current load circuit is mirrored by each of the plurality of gain cells.

Claims 28-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vagher (US 5313172), in view of Jett et al. (US 4520324) and further in view of Tanji (US 6201443).

As per claim 28, Vagher (US 5313172) and Jett et al. (US 4520324) teach claim 27. Vagher (US 5313172) doesn't disclose that each of the current mirror circuits in each of the plurality of gain cells comprises three NMOS transistors. Tanji (US 6201443) discloses variable gain amplifier fabricated in complementary metal oxide semiconductor technology in which each of the current mirror circuits in each of the plurality of gain cells comprises three NMOS transistors. The variable gain amplifier fabricated in complementary metal oxide semiconductor technology can substitute the transistors used in the digitally switched gain amplifier for digitally controlled automatic gain control amplifier applications disclosed by Vagher (US 5313172). It would have been obvious to one of ordinary skill in the art at the time the invention was made in order to provide an inexpensive and well known standard element and in order to reduce the power consumption of the digitally switched gain amplifier disclosed by Vagher (US 5313172), to use the NMOS transistors as proposed by Tanji (US 6201443).

As per claim 29, Vagher (US 5313172), Jett et al. (US 4520324) and Tanji (US 6201443) teach claim 28. Jett et al. (US 4520324) also teach plurality of switching circuits includes an NMOS and a PMOS transistor that operate to create the positive mode and an NMOS and a PMOS transistor that operate to create the negative mode (figure 3 column 3 lines 23-28).

As per claim 31, Vagher (US 5313172) and Jett et al. (US 4520324) teach claim 24. Vagher (US 5313172) disclose that each of the current mirror circuits in each of the plurality of gain cells comprises three NPN bipolar transistors. Vagher (US 5313172)

doesn't disclose that each of the current mirror circuits in each of the plurality of gain cells comprises three NMOS transistors. Tanji (US 6201443) discloses variable gain amplifier fabricated in complementary metal oxide semiconductor technology in which each of the current mirror circuits in each of the plurality of gain cells comprises three NMOS transistors. The variable gain amplifier fabricated in complementary metal oxide semiconductor technology can substitute the transistors used in the digitally switched gain amplifier for digitally controlled automatic gain control amplifier applications disclosed by Vagher (US 5313172). It would have been obvious to one of ordinary skill in the art at the time the invention was made in order to provide an inexpensive and well known standard element and in order to reduce the power consumption of the digitally switched gain amplifier disclosed by Vagher (US 5313172), to use the NMOS transistors as proposed by Tanji (US 6201443).

As per claim 32 Vagher (US 5313172) and Jett et al. (US 4520324) teach claim 24. Jett et al. (US 4520324) also teach plurality of switching circuits includes an NMOS and a PMOS transistor that operate to create the positive mode and an NMOS and a PMOS transistor that operate to create the negative mode (figure 3 column 3 lines 23-28).

Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jett et al. (US 4520324) further in view of Vagher (US 5313172) and further in view of Yun (US 6463295). Jett et al. (US 4520324) and Vagher (US 5313172) teach claim 24. Vagher (US 5313172) and Jett et al. (US 4520324) don't disclose an intermediate frequency upmixer having a intermediate frequency upmixer output coupled to an input of the

variable gain amplifier; and a radio frequency upmixer having a radio frequency upmixer input to an output of the variable gain amplifier. Yun (US 6463295) discloses an intermediate frequency upmixer (figure 1 block 157, column 17 line 31) having a intermediate frequency upmixer output coupled to an input of the variable gain amplifier (figure block 159, column 17 line 33); and a radio frequency upmixer having a radio frequency upmixer input to an output of the variable gain amplifier (figure 1 block 167, column 17 line 40). The variable gain amplifier described by Vagher (US 5313172) and Jett et al. (US 4520324) can be incorporated in the transmitter chain described by Yun (US 6463295). It would have been obvious to one of ordinary skill in the art at the time the invention was made in order to provide an inexpensive and well known standard element and in order to reduce the power consumption of the variable gain amplifier disclosed by Yun (US 6463295), to use the switched variable gain amplifier disclosed by Vagher (US 5313172) and Jett et al. (US 4520324).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Khoury et al. (US 5867778) title "Switched gain element" discloses a switched gain element that has an input differential transistor pair and a gain control stage formed of a transistor quad. The four transistors of the transistor quad are connected through respective impedances to a supply voltage. The junction of the impedances and the transistors are connected through further respective transistors to output terminals. The further transistors are switched on by respective control voltages applied to switchable current sources. The same control voltages are applied to the

transistor quad. Thus, when first predetermined voltages are applied a first voltage corresponding to the value of two of the impedances is output and when second predetermined voltages are applied a second voltage corresponding to the value of the remaining two impedances is output. The invention may also be applied to a mixer for switching the gain.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAT 11-23-2004

M. Ghayour

MOHAMMED GHAYOUR
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